rldesign.beyondP Beyond proportional design

Using proportional design, the closed-loop poles are restricted to the root locus. Often the root locus does not pass through the closed-loop pole location specified by performance requirements. Therefore, design techniques that can move the poles to desirable locations are indicated.

We consider two classes of controller: **proportional-integral-derivative (PID)** and **proportional-lead-lag**. PID controllers use "ideal" integrators (s^{-1}) and differentiators (s) and therefore require active circuits for instantiation. Proportional-lead-lag controllers can be considered approximations of PID controllers, and these can be realized in passive circuits.[1]

proportional-integral-derivative (PID) control

proportional-lead-lag control

We will build controllers incrementally by **cascade compensation**, which is illustrated in Fig. beyondP.1. This means we will begin with proportional controller design, then add cascade compensation to achieve different performance requirements. For instance, we will begin with a gain (P) control design, then cascade an integral compensator (now the controller is PI), and finally cascade a derivative compensator (now it is PID).

1. When describing "active" and "passive" controllers, we have in mind analog circuit instantiations. However, the vast majority of modern controllers are actually instantiated in *digital* circuits via *microcontrollers*. Due to the high rates of analog-to-digital (ADC) and digital-to-analog (DAC) conversion in modern controllers, often digital controller performance is nearly identical to that of a corresponding analog controller. A consequence of this is that continuous-time (analog) controller design, as we learn in this chapter, can be applied in the discrete-time (digital) case with minor alteration.

cascade compensation

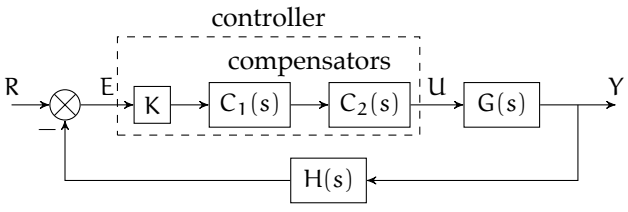

Figure beyondP.1: block diagram illustrating cascade compensation via compensators C_1 and C_2.