Resource R14 Analog input and output

Resource R14.6 Analog initialization

For our project, we will use the analog input channel CIO and the analog output channel COO on Connector C. They communicate with the processor through the FPGA.

Before they can be used, they must be initialized using

```
AIO_initialize(&CI0, &CO0);
```

Call it once, where CIO and COO are structures that must be of type $MyRio_Aio$. This initialization function is included in the me477 library.

```
Resource R14.7 Analog-to-digital converter
```

The single-channel 12-bit analog-to-digital converter (ADC) measures the current value of the applied voltage in the range [-10.000, +9.995] V. Voltages outside that range *saturate* the conversion as shown in Figure 06.5.

input saturation

The ADC has a resolution of 4.883 mV, with absolute accuracy of ± 200 mV. Each channel has input impedance of > 500 k Ω and overload protection of ± 16 V.

Our library contains a function that reads a specified channel of the ADC and returns the converted value. Its prototype is:

double Aio_Read(MyRio_Aio* channel);

where channel is the pointer to the channel structure defined above: ${\tt \&CI0}.$



Figure 06.5: ADC saturation.





Resource R14.8 Digital-to-analog converter

The single-channel 12-bit digital-to-analog converter (DAC) produces a voltage at the output terminal in the range [-10.000, +9.995] V. Again, specified voltages outside that range saturate the conversion as shown in Figure 06.6.

The DAC has a resolution of 4.883 mV, with absolute accuracy ± 200 mV. Each channel has a maximum drive current of 3 mA, a maximum slew rate of 2 V/µs, and an overload protection of ± 16 V.

Our library contains a function that accepts a specified channel for the DAC, and returns the converted value. Its prototype is:

void Aio_Write(MyRio_Aio* channel, double value);

where channel is the pointer to the channel structure defined above: &COO and value is the specified value of the analog output voltage.

RH