Now to find v_{out} . It's a voltage divider:

$$V_e = v_{\text{out}} = \frac{R_2}{R_1 + R_2} V_s.$$

The Norton equivalent is shown. We know R_e from the Thévenin equivalent, which also yields

$$I_e = V_e / R_e.$$



Figure 1.7. The Norton equivalent circuit.

1.5 Output and Input Resistance and Circuit Loading

When considering a circuit from the perspective of two terminals either as *input* or *output*—it is often characterized as having a



Thévenin/Norton **equivalent resistance** and, if it is considered as an output, as having an equivalent (Thévenin or Norton) source.

If the terminals are considered to be an *output*, its **output resistance** is just the Thévenin/Norton equivalent resistance. Other names for this output resistance are *source* or *internal resisistance*.³ Figure 1.8 illustrates this model.

3. Sometimes, instead of *resistance*, the term *impedance* is substituded. In these situations, there is no difference in meaning.



Figure 1.8. Source with Thévenin equivalent source voltage V_e and output/internal resistance R_e and a load with input resistance R_L .

If the terminals are considered to be an *input*, its **input resistance** is the is the Thévenin/Norton equivalent resistance of the circuit. Another term for this input resistance is the *load resistance*.

1.5.1 Loading the Source

Loading a source means to connect another circuit to it that draws power. Let's explore what happens when we connect the load to the source for the circuit in figure 1.8.

Before connecting, the source output voltage is

$$v_{\text{out}} = V_e - v_{R_e}$$
$$= V_e - \oint_{R_e} R_e$$
$$= V_e.$$

This is equivalent to connecting a load with an infinite resistance. After connecting, we have a voltage divider, so

$$v_{\text{out}} = \frac{R_L}{R_e + R_L} V_e$$
$$= \frac{1}{1 + R_e / R_L} V_e.$$

So, as $R_e/R_L \rightarrow 0$, $v_{out} \rightarrow V_e$. Also, as $R_e/R_L \rightarrow \infty$, $v_{out} \rightarrow 0$.

So, relatively small output resistance and large input resistance yield a "loaded" voltage nearer nominal. Some sources are labeled with nominal values assuming no

load and others assuming a **matching load**⁴—a load equal to the output impedance. For this reason, it is best to measure the actual output of any source.

1.6 Capacitors

Capacitors have two terminal and are composed of two conductive surfaces separated by some distance. One surface has charge q and the other -q. A capacitor stores energy in an *electric field* between the surfaces.

Let a capacitor with voltage v across it and charge q be characterized by the parameter **capacitance** *C*, where the constitutive equation is

q = Cv.

The capacitance has derived SI unit **farad (F)**, where $F = A \cdot s/V$. A farad is actually quite a lot of capacitance. Most capacitors have capacitances best represented in μ F, nF, and pF.

The time-derivative of this equation yields the *v-i* relationship (what we call the "elemental equation") for capacitors. capacitor elemental equation A time-derivative! This is new. Resistors have only algebraic *i-v* relationships, so circuits with only sources and resistors can be described by *algebraic* relationships. The dynamics of circuits with capacitors are described with *differential equations*.



Figure 1.9. capacitor circuit diagram symbols.

Capacitors allow us to build many new types of circuits: filtering, energy storage, resonant, blocking (blocks dc-component), and bypassing (draws ac-component to ground).

Capacitors come in a number of varieties, with those with the largest capacity (and least expensive) being **electrolytic** and most common being **ceramic**. There are two functional varieties of capacitors: **bipolar** and **polarized**, with circuit diagram symbols shown in figure 1.9. Polarized capacitors can have voltage drop across in only one direction, from **anode** (+) to **cathode** (–)—otherwise they are damaged or may **explode**. Electrolytic capacitors are polarized and ceramic capacitors are bipolar.

4. A matching load can be shown to have maximum power transfer.

