1. just use $R_{d_i} = 0$ or
2. use some reasonably central value of $\overline{v}_{D_i} > 0.6$ V.

The second case is preferred if $v_{D_i}(t)$ spends much time above 0.6 V. But usually, if it spends much time, the mean $\overline{v}_{D_i}$ should be great enough to avoid this situation. Circuits that tend to express this behavior are those with high impedance and correspondingly low currents.

4.3 MOSFETs

A metal–oxide–semiconductor field-effect transistor (MOSFET) is a *two-port*, *nonlinear* circuit element that lies at the heart of digital electronics, with sometimes millions integrated into a single microprocessor. They are the dominant type of **transistor**, a class of elements that includes the **bipolar junction transistor (BJT)**.

MOSFETs are not just common in integrated circuits made of silicon, they are also available as discrete elements, which is the form most often encountered by the mechatronicist.

There are two primary types of MOSFET: the **n-channel** and the **p-channel**, determined by the type of semiconductor doping (negative or positive) used in the manufacturing process. These types are "opposites," so we choose to focus on n-channel, here.

Figure 4.8 displays the circuit diagram symbol for the MOSFET. There are three[4] terminals: the **gate** G, **drain** D, and **source** S. The current flowing from one terminal to another is labeled with consecutive subscripts; for instance, the current flowing from drain to source is i_{DS}. Similarly, the voltage drop across two terminals is labeled with concurrent subscripts; for instance, the voltage drop from gate to source is v_{GS}.

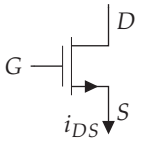


Figure 4.8. Circuit symbol for a n-channel MOSFET.

The input-output characteristics of the MOSFET are quite complex, but we may, in the first approximation, consider it to be like a *switch*. In this model, called the

4. Note that if we consider the gate-side to be the input with $i_{GS} = 0$ and v_{GS} and the drain-source-side to be the output with i_{DS} and v_{DS}, the MOSFET can be seen to be two-port.

S-model, if the gate voltage v_{GS} is less than the **threshold voltage** V_T (typically around 0.7 V), the D and S terminals are disconnected (open) from each other (OFF mode). But when $v_{GS} > V_T$, D and S are connected via a short and current i_{DS} can flow (ON mode).

The input-output characteristics of a MOSFET are actually much more complex than the S-model captures. The S-model can build intuition and suffice for digital logic circuit analysis. However, we are here mostly concerned with analog circuit models. Specifically, we mechatronicists use MOSFETs to drive power-hungry loads (e.g. motors) with high-power sources controlled by low-power microcontrollers. We now turn to a general model, after which we consider a method of analyzing MOSFET circuits.

4.3.1 The Switch Unified (SU) Model

The **switch unified (SU) model** is reasonably accurate at describing actual MOSFET input-output characteristics. However, it is quite *nonlinear*, and therefore can give us headaches during analysis. As usual, we are concerned with the element's voltage-current relationships.

Definition 4.4

Let K be a constant parameter of the MOSFET with units A/V^2. K can be found from parameters of a given MOSFET. The current into the gate is zero: $i_G = 0$. The current from drain to source is controlled by the two voltage variables v_{GS} and v_{DS}, as shown.

$$i_{DS} = \begin{cases} 0 & \text{for } v_{GS} < V_T \\ K\left((v_{GS} - V_T)v_{DS} - v_{DS}^2/2\right) & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} < v_{GS} - V_T \\ \dfrac{K}{2}(v_{GS} - V_T)^2 & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} \geq v_{GS} - V_T \end{cases}$$

So, as in the S-model, the gate voltage v_{GS} must exceed the threshold voltage V_T for current to flow. The interval below the threshold is called the **cutoff region** (OFF). Note, however, that current doesn't just flow freely, as it would with the short of the S-model. In fact, two distinct ON ($v_{GS} > V_T$) intervals emerge. In both, the current i_{DS} depends on v_{GS}. In the **triode region**, $v_{DS} < v_{GS} - V_T$, i_{DS} also depends on v_{DS}. However, in the **saturation region**, $v_{DS} > v_{GS} - V_T$, i_{DS} is independent of v_{DS} and can be controlled by v_{GS}, alone.

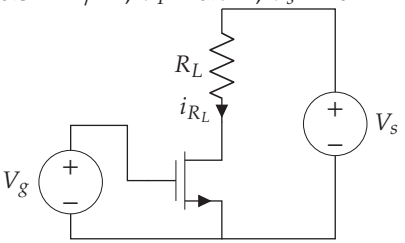
Note that in saturation, the MOSFET behaves like a current source controlled by v_{GS}. A source controlled by a variable in the circuit is called a **dependent source**. This behavior as a dependent current source (that can also be turned off) is the most valuable for us.

The **switch current source (SCS) model** is actually just a recognition of this behavior and an elimination of the triode region from consideration. This is a reasonable assumption if we can guarantee operation in cutoff or saturation only.

Given the piecewise MOSFET models, we can again use the **method of assumed states** for MOSFET circuit analysis. Note however that only the S-model is piecewise linear and that the SU- and SCS-models are piecewise nonlinear. We can handle some relatively simple nonlinear cases analytically, but require either linearization or numerical assistance for more complex circuit analyses.

Example 4.3

Given the circuit shown, solve for the voltage across the load R_L for varying V_g given the following conditions: saturation of the MOSFET, $R_L = 1$ kΩ, $K = 0.5$ mA/V^2, $V_T = 0.7$ V, $V_s = 10$ V.



During saturation,

$$i_{DS} = \frac{K}{2}(v_{GS} - V_T)^2.$$

We know that $v_{GS} = V_g$ and the other parameters are given. The voltage across the resistor is, from Ohm's law,

$$v_{R_L} = i_{R_L} R_L.$$

From KCL,

$$\begin{aligned} v_{R_L} &= i_{DS} R_L \\ &= \frac{KR_L}{2}(V_g - V_T)^2. \end{aligned}$$

This is our load voltage, but we must determine the range of V_g for which saturation is satisfied. We must first find v_{DS}. From KVL,

$$\begin{aligned} v_{DS} &= V_s - v_{R_L} \\ &= V_s - \frac{KR_L}{2}(V_g - V_T)^2. \end{aligned}$$

The condition for saturation (in addition to $V_g > V_T$) is

$$v_{DS} \geq v_{GS} - V_T \quad \Rightarrow$$

$$V_s - \frac{KR_L}{2}(V_g - V_T)^2 \geq V_g - V_T \quad \Rightarrow$$

$$V_T - \frac{1 + \sqrt{2KR_L V_s}}{KR_L} \leq V_g \leq V_T + \frac{-1 + \sqrt{2KR_L V_s}}{KR_L}.$$

Since $V_g > V_T$, we can simplify the condition for saturation to

$$V_T < V_g \leq V_T + \frac{-1 + \sqrt{2KR_L V_s}}{KR_L}.$$

Computing the upper bound, we obtain 5.33 V. See figure 4.9 for the plot. Note that the similar input and load voltage might suggest we didn't need to MOSFET. However, the input voltage has virtually zero load, whereas the source voltage does. Essentially, the current draw (and therefore power) is different! We're controlling a constant, more powerful source with a weaker, (ideally) variable source.

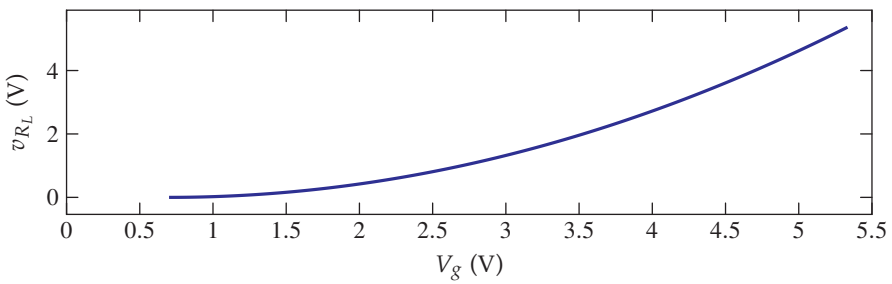


Figure 4.9. The load voltage as a function of gate voltage.

4.4 Operational Amplifiers

The **operational amplifier** (opamp) is the queen of analog electronic components. The opamp is a *four-port nonlinear* voltage-controlled voltage source, but it's so much more. Here are a few applications from the opamp highlight reel: summing two signals, subtracting two signals, amplifying a signal, integrating a signal, differentiating a signal, filtering a signal, isolating two subcircuits, generating periodic functions (e.g., sinusoids and square waves), and analog feedback control. Although they are nonlinear, in most applications a linear approximation is sufficiently accurate.

Figure 4.10 shows the circuit symbol for the opamp. Three terminals are displayed:

inverting input (−) The **inverting input** is labeled with the "−" symbol.
non-inverting input (+) The **non-inverting input** is labeled with the "+" symbol.
output The **output** extends from the tip of the symbol, opposite the inputs.

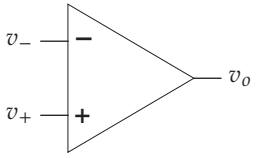


Figure 4.10. Circuit symbol for an opamp.

These comprise an input and an output port. However, there are two power supply ports that are typically suppressed in the circuit diagram. These two power supply ports are from a **differential supply**, which has a positive terminal (e.g., +12 V), symmetrically negative terminal (e.g., −12 V), and a common ground. The supply provides the opamp with external power, making it an **active** element.

When an opamp is operating in its linear mode, it outputs a voltage v_o that is A times the difference between its inputs v_+ and v_-. The **open-loop gain** A is different for every opamp, but is usually greater than 10^5. Let's formalize this model.

Definition 4.5

An opamp's input terminals + and − draw zero current (i.e. have infinite input impedance). Let A be a positive real number. The output voltage v_o is given by

$$v_o = A(v_+ - v_-).$$

The output terminal has zero impedance.